CLAIMS

What is claimed is:

1. A bipolar transistor comprising:

a conductive back electrode for receiving a bias voltage;

an insulating layer located over said conductive back electrode;

a first semiconductor layer located over said insulating layer, said first semiconductor layer comprising a base which includes a first conductive type dopant and an extrinsic collector which includes a second conductivity type dopant, said extrinsic collector borders said base; and

an emitter comprising a second semiconductor layer of the second conductivity type dopant located over a portion of said base, wherein said conductive back electrode is biased to form an inversion charge layer in said base region at an interface between said first semiconductor layer and said insulating layer.

2. The bipolar transistor of Claim 1 wherein a portion of said base is a doped to form an extrinsic base.

3. The bipolar transistor of Claim 2 wherein the extrinsic base, the emitter, the extrinsic collector and the exposed surfaces of the conductive back electrode each include a silicide.

4. The bipolar transistor of Claim 3 wherein the silicide is in contact with a metal contact that is located atop the silicide inside a contact opening formed in an interconnect dielectric.

5. The bipolar transistor of Claim 1 wherein the emitter comprises a single-finger.

6. The bipolar transistor of Claim 1 wherein the emitter comprises multi-fingers.

7. The bipolar transistor of Claim 2 wherein the extrinsic collector and the extrinsic base are raised regions.

8. The bipolar transistor of Claim 1 wherein a spacer is located on sidewalls of the emitter.

9. The bipolar transistor of Claim 1 wherein said insulating layer is a thin insulating layer having a thickness from about 1 to about 15 nm.

10. The bipolar transistor of Claim 9 wherein another insulating layer that is thicker than the thin insulating layer is located adjacent thereto, said another insulating layer is a buried oxide of a silicon-on-insulator.

11. The bipolar transistor of Claim 2 wherein the base contains a p-type dopant, the emitter contains an n-type dopant, the extrinsic collector contains an n-type dopant and the extrinsic base contains a p-type dopant.

12. The bipolar transistor of Claim 2 wherein the extrinsic base diffuses minimally into the base so as not to be in contact with the underlying insulating layer.

13. An integrated semiconductor structure comprising

a bipolar transistor comprising a conductive back electrode for receiving a bias voltage; an insulating layer located over said conductive back electrode; a first semiconductor layer located over said insulating layer, said first semiconductor layer comprising a base which includes a first conductive type dopant and an extrinsic

collector which includes a second conductivity type dopant, said extrinsic collector borders said base; and an emitter comprising a second semiconductor layer of the second conductivity type dopant located over a portion of said base region, wherein said conductive back electrode is biased to form an inversion charge layer in said base region at an interface between said first semiconductor layer and said insulating layer; and

at least one adjacent complementary metal oxide semiconductor device, said bipolar transistor and said at least one adjacent complementary metal oxide semiconductor device are separated by an isolation region.

14. The integrated semiconductor structure of Claim 13 wherein the complementary metal oxide semiconductor device is a field effect transistor.

15. A method of fabricating a bipolar transistor comprising the steps of:

providing a silicon-on-insulator (SOI) substrate comprising a first semiconductor layer located over a first insulating layer, wherein a portion of the first insulating layer beneath said first semiconductor layer is removed providing an undercut region;

forming a second insulating layer on exposed surfaces of said first semiconductor layer, wherein said second insulating layer is thinner than said first insulating layer;

filling the undercut region and the removed portion of the first semiconductor layer with a conductive back electrode material;

forming an extrinsic base containing a first conductivity dopant and an extrinsic collector containing a second conductivity type dopant in portions of the first semiconductor layer;

forming an emitter comprising a second semiconductor layer including said second conductivity type dopant over a portion of said first semiconductor layer; and

biasing the conductive back electrode material to form an inversion charge layer at an interface between the first semiconductor layer and the second insulating layer.

16. The method of Claim 15 wherein said providing the SOI substrate comprises forming a trench into the first semiconductor layer, stopping on said first insulating layer; and performing an isotropic etch process to form said undercut region.

17. The method of Claim 15 wherein said forming the second insulating layer comprises a thermal growth process.

18. The method of Claim 15 wherein said filling the undercut region comprises depositing a doped polysilicon layer.

19. The method of Claim 15 wherein said extrinsic collector is formed by forming a patterned mask on at least a portion of the first semiconductor layer and ion implanting into exposed portions of the first semiconductor layer, and said extrinsic base is formed by forming a patterned mask on at least a portion of the first semiconductor layer and ion implanting into exposed portions of the first semiconductor layer.

20. The method of Claim 15 wherein the extrinsic base contains a p-type dopant and the extrinsic collector contains an n-type dopant, wherein the dopants are introduced via separate ion implantation processes.

21. The method of Claim 15 wherein the forming the emitter includes the step of forming a dummy emitter on the first semiconductor layer, forming spacers about the dummy emitter, forming an etch stop layer and a planarizing material, planarizing the planarizing material to expose a surface of the etch stop layer atop the dummy emitter, removing the exposed etch stop layer, removing at least the dummy emitter providing an emitter opening that exposes the first semiconductor and depositing said second semiconductor layer to fill said emitter opening.

22. The method of Claim 21 further comprising forming a hardmask on the second semiconductor layer and patterning the hardmask and the second semiconductor layer.

23. The method of Claim 22 further comprising etching back at least said planarizing material, said hardmask and said etch stop layer exposing said emitter and surfaces of said first semiconductor layer wherein said extrinsic collector and extrinsic base are located.

24. The method of Claim 23 further comprising forming a silicide on at least said emitter, said extrinsic collector and said extrinsic base utilizing a silicidation process.

25. The method of Claim 24 further comprising forming an interconnect dielectric having a contact opening that exposes said silicide; and filling said contact opening with a contact metal.

26. The method of Claim 15 wherein said biasing is performed using an external source.

27. The method of Claim 15 further comprising forming spacers about said emitter, said spacers being formed prior to emitter formation using a dummy emitter process.

28. The method of Claim 15 further comprising forming trench isolation regions on top of portions of said first insulating layer.

29. The method of Claim 15 wherein the extrinsic base is formed with minimal diffusion of said dopant thereby said extrinsic base is not in contact with said second insulating layer.

30. The method of Claim 15 further comprising forming raised extrinsic collector and extrinsic base regions.

31. The method of Claim 15 wherein the undercut region is provided by an isotropic etching process in which no pad layers are present on said first semiconductor layer.